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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,560	01/16/2001	Kenny Kok-Hoong Chiu	052404.0098	3810

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EXAMINER	
WILLIAMS, LAWRENCE B	
ART UNIT	**PAPER NUMBER**
2634	6

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,560	CHIU, KENNY KOK-HOONG	
	Examiner	Art Unit	
	Lawrence B Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13-23 and 27-38* is/are rejected.

7)☒ Claim(s) *10-12, 24-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 13-17, 27-32 and 34-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Watt (US Patent 5,675,615).

(1) With regard to claim 1, Watt discloses in Fig. 5, a clock selection device adapted to select one of a pair of clock sources onto an output clock line, comprising: a first input clock line (mclk) coupled to a first clock source; a second input clock line (fclk) coupled to a second clock source, the second clock source asynchronous to the first clock source (col. 5, lines 46-50); and a clock selection logic (28) adapted to select from the first input clock line and the second input clock line, producing an internal clock line coupled to the output clock line (col. 6, lines 47-63).

(2) With regard to claim 2, Watt also discloses, the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency (abstract).

(3) With regard to claim 3, Watt also discloses in Fig. 5, the clock selection device of claim 1, further comprising: a clock synchronization logic (Synchroniser Cir) coupled to the first input clock line, the second input clock line, and the clock selection logic, adapted to synchronize the first input clock line, the second input clock line, and the clock selection logic, such that the internal clock line is glitch free (col. 4, lines 12-20).

(4) With regard to claim 4, Watt also discloses the clock selection device of claim 3, the clock synchronization logic comprising: a first clock synchronization block (Synchroniser Cir), coupled to the first clock source, adapted to synchronize the first clock source and the clock selection logic; and a second clock synchronization block, coupled to the second clock source (Synchroniser Cir), adapted to synchronize the second clock source and the clock selection logic.

(5) With regard to claim 13, Watt also discloses in Fig. 5, a buffer (24) coupled to the internal clock line, producing a buffered output clock signal.

(6) With regard to claim 14, claim 14 inherits all limitations of claim 1 above (col. 7, lines 60-67).

(7) With regard to claim 15, Watt also discloses, the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency (abstract).

(8) With regard to claim 16, Watt also discloses in Fig. 5, the clock selection device of claim 1, further comprising: a clock synchronization logic (Synchroniser Cir) coupled to the first input clock line, the second input clock line, and the clock selection logic, adapted to synchronize the first input clock line, the second input clock line, and the clock selection logic, such that the internal clock line is glitch free (col. 4, lines 12-20).

(9) With regard to claim 17, Watt also discloses the clock selection device of claim 3, the clock synchronization logic comprising: a first clock synchronization block (Synchroniser Cir), coupled to the first clock source, adapted to synchronize the first clock source and the clock selection logic; and a second clock synchronization block, coupled to the second clock source (Synchroniser Cir), adapted to synchronize the second clock source and the clock selection logic.

(10) With regard to claim 27, Watt also discloses in Fig. 5, a buffer (24) coupled to the internal clock line, producing a buffered output clock signal on the output clock line.

(11) With regard to claim 28, claim 28 inherits all limitations of claims 1 and 14 above.

(12) With regard to claim 29, claim 29 inherits all limitations of claim 28. Furthermore, Watt also discloses the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency (abstract).

(13) With regard to claim 30, Watt also discloses in Fig. 5, buffering (24) the internal clock line to generate the output clock line.

(14) With regard to claim 31, claim 31 inherits all limitations of claims 16 and 28.

(15) With regard to claim 32, Watt also discloses the delaying step of claim 31 for a predetermined amount of time (abstract).

(16) With regard to claim 34, Watt also discloses the method of claim 28, step (c) comprising the steps of (cl) receiving a clock select signal asynchronous to the first clock signal and the second clock signal; and (c2) connecting the first clock signal to the output clock line when the clock select signal is asserted; (c3) connecting the second clock signal to the output clock line when the clock select signal is deasserted; (c4) synchronizing the first input clock signal, the second input clock signal, and steps (c2) and (c3), such that the output clock line is

glitch free (col. 3, lines 14-42).

(17) With regard to claim 35, claim 35 inherits all limitations of claims 1, 3, 14, 28.

(18) With regard to claim 36, claim 36 inherits all limitations of claims 5 and 36 above.

(19) With regard to claim 37, Watt also discloses the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency (abstract).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 5-9, 18-23, 33, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watt (US Patent 5,675,615) as applied to claims 1, 3, 4, 14, 31, 35 above, and further in view of Chesavage (US Patent 6,239,626 B1).

(1) With regard to claim 5, as noted above, Watt discloses all limitations of claim 4. Watt does not however disclose the clock synchronization logic further comprising: a first clock reset signal, synchronized to the first clock signal, adapted to reset the first clock synchronization block; and a second clock reset signal, synchronized to the second clock signal, adapted to reset the second clock synchronization block, wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic.

However, Chesavage discloses in Fig. 4, a clock selector with clock synchronization logic further comprising: a first clock reset signal (84a), synchronized to the first clock signal, adapted to reset the first clock synchronization block; and a second clock reset signal (84b), synchronized to the second clock signal, adapted to reset the second clock synchronization block, wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic (col. 2, lines 25-42).

One skilled in the art would have clearly recognized a clock selector with clock synchronization logic further comprising: a first clock reset signal, synchronized to the first clock signal, adapted to reset the first clock synchronization block; and a second clock reset signal, synchronized to the second clock signal, adapted to reset the second clock synchronization block, wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic is a well-known technique introduced in many references. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Chesavage to modify the invention of Watt as a method of selecting clock sources in a glitch-free manner (col. 2, lines 12-21).

(2) With regard to claim 6, Chesavage also discloses the clock selection device wherein the clock synchronization logic is scalable to produce a predetermined delay time between the assertion of the clock select signal and the selection onto the output line by the clock selection logic (col. 5, line 66 – col. 6, line 13).

(3) With regard to claim 7, Chesavage also discloses in Fig. 4, wherein the clock selection logic comprises a multiplexer (90) with two clock input lines.

(4) With regard to claim 8, claim 8 is rejected under 35 U.S.C. 103(1) as being

unpatentable over Chesavage (US Patent 6,239,626 B1).

Although Chesavage doesn't specifically disclose, "wherein the multiplexer switches only when both clock input lines of the multiplexer are at the same assertion level", such a limitation is a matter of design choice and would have been obvious in the system of Chesavage. The limitation in claim 8 does not define a patentably distinct invention over that of Chesavage as a whole since both the invention and Chesavage are directed to a "glitch-free clock selection". The multiplexer switching only when both clock input lines are at the same assertion level is inconsequential for the invention as a whole and presents no new or unexpected results, so long as glitch-free clock selection is achieved. Therefore "having the multiplexer switch clocks only when both of its input lines are at the same assertion level" would have been a matter of obvious design choice to one of ordinary skill in the art.

(5) With regard to claim 9, Chesavage also discloses in Fig. 4, the clock selection device of claim 1, further comprising: a clock selection signal (98), asynchronous to the first clock source and the second clock source, adapted to cause the clock selection logic to select one of the first input clock source and the second input clock source onto the internal clock line, selecting the first input clock source when the clock selection signal is asserted and the second input clock source when the clock selection signal is deasserted (col. 4, lines 29-62).

(6) With regard to claim 18, Chesavage discloses in Fig. 4, a clock selector with clock synchronization logic further comprising: a first clock reset signal (84a), synchronized to the first clock signal, adapted to reset the first clock synchronization block; and a second clock reset signal (84b), synchronized to the second clock signal, adapted to reset the second clock

synchronization block, wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic (col. 2, lines 25-42).

(7) With regard to claim 19, Chesavage also discloses the clock selection device wherein the clock synchronization logic is scalable to produce a predetermined delay time between the assertion of the clock select signal and the selection onto the output line by the clock selection logic (col. 5, line 66 – col. 6, line 13).

(8) With regard to claim 20, Chesavage also discloses in Fig. 4, wherein the clock selection logic comprises a multiplexer (90) with two clock input lines.

(9) With regard to claim 21, claim 21 inherits all limitations of claims 8 and 20 above.

(10) With regard to claim 22, Chesavage also discloses in Fig. 4, the clock selection device of claim 1, further comprising: a clock selection signal (98), asynchronous to the first clock source and the second clock source, adapted to cause the clock selection logic to select one of the first input clock source and the second input clock source onto the internal clock line, selecting the first input clock source when the clock selection signal is asserted and the second input clock source when the clock selection signal is deasserted (col. 4, lines 29-62).

(11) With regard to claim 23, claim 23 inherits the limitations of claim 22. Furthermore, Watt discloses a clock synchronization logic (Synchroniser Cir) coupled to the first input clock line, the second input clock line, and the clock selection logic, adapted to synchronize the first input clock line, the second input clock line, and the clock selection logic, such that the internal clock line is glitch free (col. 4, lines 12-20).

(12) With regard to claim 33, claim inherits all limitations of claim 31 above. Furthermore, Chesavage discloses in Fig. 5, resetting a synchronization logic (Synchroniser cir)

with a first reset signal synchronous to the first clock signal; and resetting the synchronous logic with a second reset signal synchronous to the second signal.

(13) As noted above, claim 38 inherits all limitations of claim 35, above. Furthermore, Watt also discloses the clock switching mechanism of claim 35, the clock synchronization means comprising: a first synchronization means (44) coupled to the first clock source for synchronizing the first clock source (mclk) to the clock switching means; a second synchronization means (46) coupled to the second clock source (fclk) for synchronizing the second clock source to the clock switching means; a clock selection means coupled to the first synchronization means and the second synchronization means for causing the clock switching means to switch between the first clock source and the second clock source. Chesavage discloses in Fig. 4, a first feedback means coupled to the clock selection means (98) and the first synchronization means (88a) for synchronizing the second synchronization means and the clock selection means; and a second feedback means coupled to the clock selection means and the second synchronization means (88b) for synchronizing the first synchronization means and the clock selection means.

Allowable Subject Matter

6. Claims 10-12, and 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 703-305-6969. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
April 9, 2004

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